NISIN

触摸显示模组产品规格承认书

Displaly Module Specifications for Approval

客户： 客户型号：					
批准 APPROVED	审核 CHECKED	拟制 DESIGNED	批准 APPROVED	审核 CHECKED	拟制 DESIGNED

R-R-020-A0

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1.产品规格（Product Specifications）

面板类型（Panel Type）	TFT LCD
面板尺寸(Panel Size)	7 inch
显示类型（Display Type）	Normal Black
分辨率（Resolution）	800 (RGB) x 1280 (dot)
显示点间距（Dot Pitch）	39.25um X 117.75um
显示色彩（color）	16.7M
视角（View Angle）	U/D/L/R: 80/80/80/80
显示驱动 IC（Display Driver IC）	ILI9881C
接口类型（Interface Type）	MIPI
触摸类型（TP Type）	外挂 TP
触摸 IC （TP IC）	GT1151QM
外形尺寸（Dimensions）	124(H) X 181 (V) X 5.21(T)(mm)
显示区尺寸（Display area）	94.2X 150.72(mm)
模组亮度（Module Brightness）	300cd/m²
触摸点数 Touch points	10
触摸按键 Touch Key Number	0
触摸屏固件版本	Version:

2.产品图纸（Product Drawings）

见 CAD 图纸

3. 接口定义（The Interface Definition）

见 CAD 图纸

4.电性特性（Electrical Characteristics）

18. Electrical Characteristics

18.1. Absolute Maximum Ratings

The absolute maximum rating is listed in Table 36. When the ILI9881C is used out of the absolute maximum ratings, it may be permanently damaged. To use the ILI9881C within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ILI9881C will malfunction and cause poor reliability.

Table 36: Absolute Maximum Ratings

Item	Symbol	Unit	Value
Analog Operating Voltage	VCI ~ GND	V	-0.3 ~ +6.5
Analog Operating Voltage	VCIREF ~ GND	V	-0.3 ~ +6.5
Digital Operating Voltage	VDDI ~ GND	V	-0.3 ~ +3.6
Digital Operating Voltage	VCC1 ~ GND	V	-0.3 ~ +6.5
Digital Operating Voltage	VCC2 ~ GND	V	-0.3 ~ +6.5
DSI Operating Voltage	VDDAM ~ GND	V	-0.3 ~ +3.6
OTP Supply Voltage	MTP_PWR ~ GND	V	-0.3 ~ +9.0
Supply Voltage	VSP ~ GND	V	-0.3 ~ +6.5
Supply Voltage	VSN ~ GND	V	0.3 ~ -6.5
Gate Driver High Voltage	VGH ~ GND	V	-0.3 ~ +18
Gate Driver Low Voltage	VGL ~ GND	V	0.3 ~ -18
Driver Supply Voltage	VCI - VCL	V	≦ 6.0V
Driver Supply Voltage	VGH - VGL	V	≦ 32.0V
Input Voltage	VIN	V	-0.3 ~ VDDI + 0.3
HS Input Voltage	VHSIN	V	-0.3 ~ + 1.65
Operating Temperature	Topr	℃	-30 ~ +70
Storage Temperature	Tstg	℃	-55 ~ +110

Note: *Even if the absolute maximum rating of one of the above parameters is exceeded only for a short while, the quality of the product may be degraded. Therefore, be sure to use the product within the range of the*

18.2. DC Characteristics for Panel Driving

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power & Operation Voltage							
Analog operating voltage	VCI	-	2.5	2.8	6.0	V	
Analog operating voltage	VCIREF		2.5	2.8	6.0		
Digital operating voltage	VDDI	-	1.65	2.8	3.3	V	
Digital operating voltage	VCC1		1.65	2.8	6.0	V	
Digital operating voltage	VCC2		1.65	2.8	6.0	V	
DSI operating voltage	VDDAM	-	1.65	1.8	3.3	V	
OTP Supply voltage	MTP_PWR	-	8.4	8.5	8.6	V	
Analog operating voltage	VSP	-	4.5		6	V	
Analog operating voltage	VSN	-	-6		-4.5	V	
Logic High level input voltage	VIH	-	0.7*VDDI		VDDI	V	Note1
Logic Low level input voltage	VIL	-	-0.3		0.3*VDDI	V	Note1
Logic High level output voltage TE , LEDPWM	VOH	IOH = -1.0mA	0.8*VDDI		VDDI	V	Note1
Logic Low level output voltage TE , LEDPWM	VOL	IOL = +1.0mA	0		0.2*VDDI	V	Note1
Gate Driver High Voltage	VGH	-	8.0	-	18	V	
Gate Driver Low Voltage	VGL	-	-18.0	-	-7.0	V	
Driver Supply Voltage	-	|VGH-VGL|	15	-	32	V	
VCOM Operation							
DC VCOM Amplitude Voltage	VCOM	-	-4.0	-	0	V	Note3
Source Driver							
Source Output Range	VSOUT(+)	-	0.3	-	VREG1OUT-0.1	V	Note4
	VSOUT(-)	-	VREG2OUT +0.1	-	-0.3	V	Note4
Positive Gamma Reference Voltage	VREG1OUT	-	2.9	-	VSP-0.5	V	
Negative Gamma Reference Voltage	VREG2OUT	-	VSN+0.5	-	-2.9	V	
Source Output Setting Time	Tr	Below with 99% precision	-	10	-	uS	Note3.4
Output Deviation Voltage (Source Output channel)	Vdev	Sout>=4.2V Sout<=0.8V	-	-	20	mV	Note3
		4.2V>Sout>0.8V	-	-	15	mV	
Output Offset Voltage	VOFFSET	-	-	-	35	mV	Note3
Standby mode current consumption							
Sleep In mode	I(VDDI SLP IN)	Ta = 25 °C VCI=2.8V VDDI=1.8V	-	35	-	uA	
	I(VCI SLP IN)		-	25	-	uA	

Notes:

1. Ta = -30 to 70 °C (to 85 °C no damage) , VCI = 2.5V to 6.0V, VDDI = 1.65V to 3.3V

2. Supply digital VDDI voltage equal or less than analog VCI voltage.

3. Source channel loading = 9KΩ,70pF/channel

4. The maximum value is between with Note 3 and Gamma setting value

18.4.3. High Speed Mode – Data Clock Channel Timing

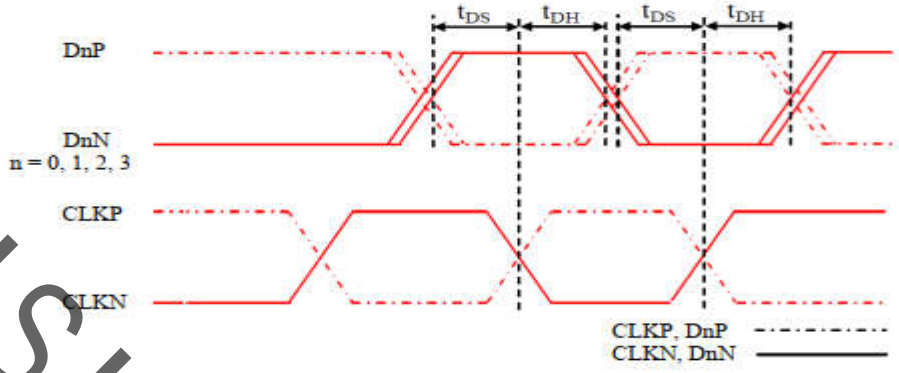


Figure 118: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

18.4. AC Characteristics

18.4.1. DSI Timing Characteristics

18.4.2. High Speed Mode – Clock Channel Timing

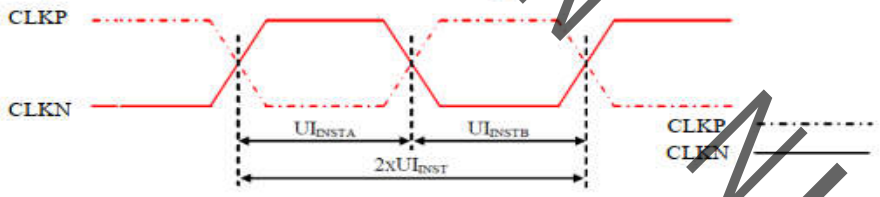


Figure 117: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
CLKP/N	UI_{INSTA},UI_{INSTB} (Note 1)	UI instantaneous Half	2 (Note 2)	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value of 24 UI per Pixel, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	433 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	487 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps

18.4.4. High Speed Mode – Rising and Falling Timings

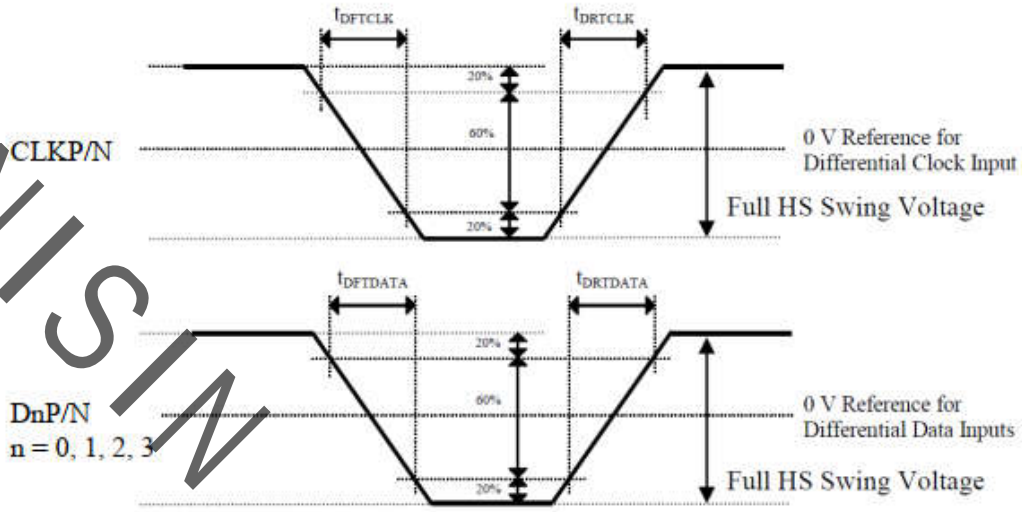


Figure 119: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

18.4.6. Data Lanes from Low Power Mode to High Speed Mode

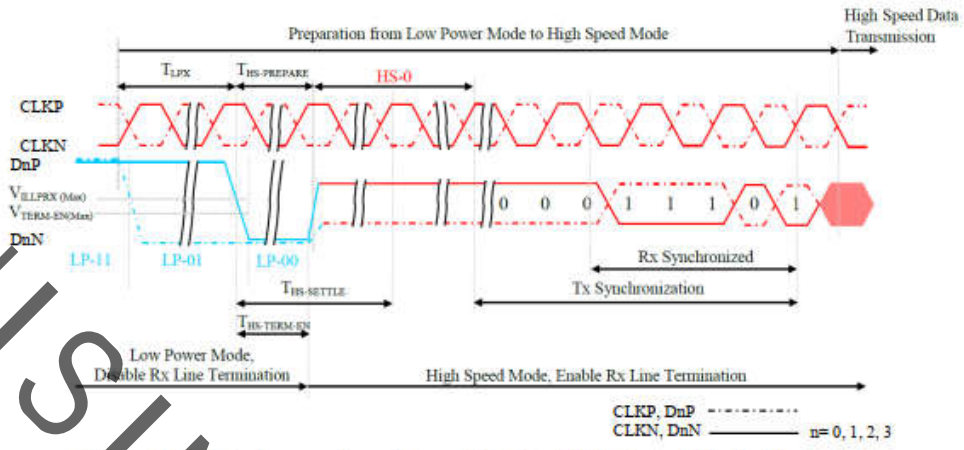
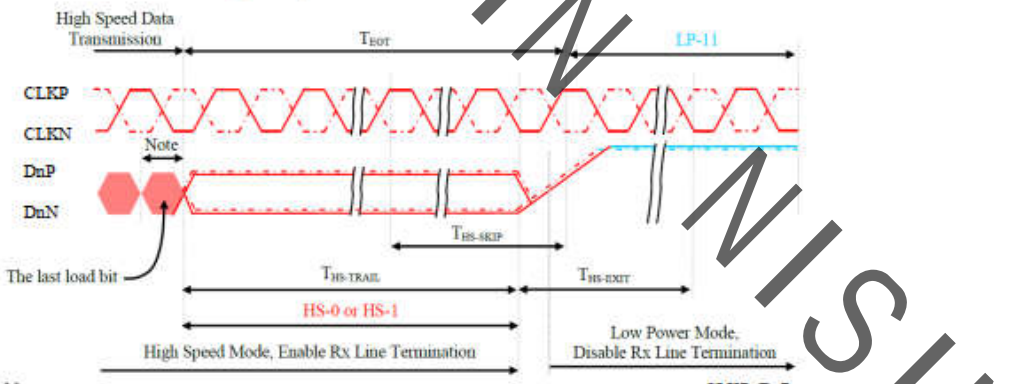


Figure 122: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

18.4.7. Data Lanes from High Speed Mode to Low Power Mode



Note:
If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.
If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

Figure 123: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

18.4.8. DSI Clock Burst – High Speed Mode to/from Low Power Mode

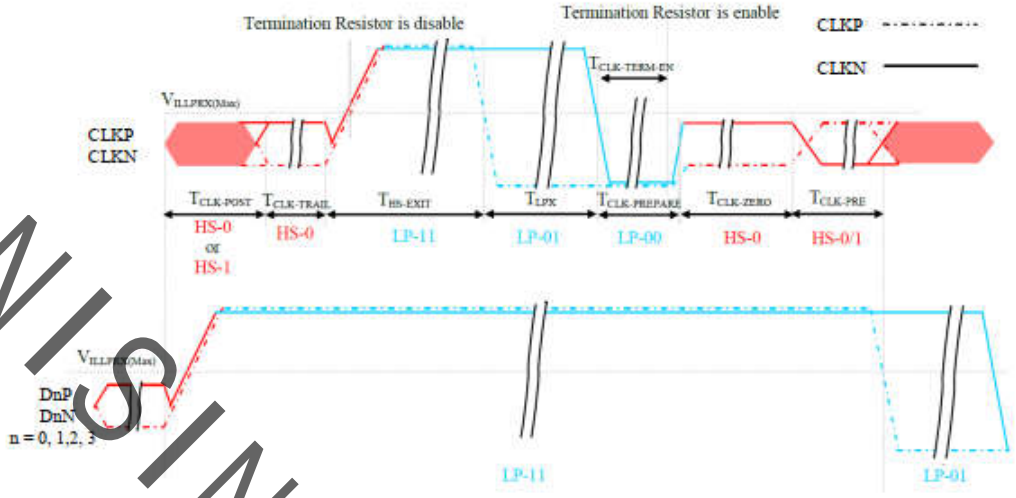


Figure 124: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

18.4.10. Reset Timing

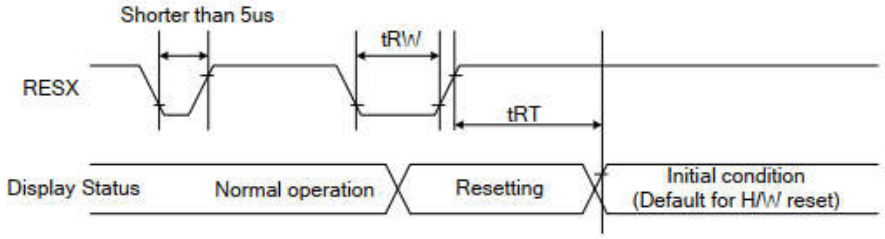


Figure 125: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Notes:

1. *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.*
2. *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.*

Table 48: Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

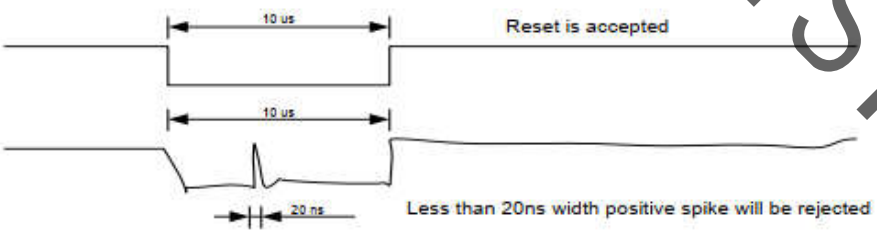
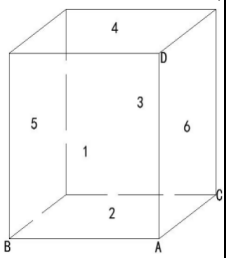


Figure 126: Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

5.可靠性实验测试(Reliability Test Conditions And Methods)

<table>
<tr><th>序号</th><th>试 验项目</th><th>试验条件及方法</th><th>试验设备</th><th>检验项目</th><th>检验工具</th></tr>
<tr><td>1</td><td>高 温高 湿(静、动 态 ）试验</td><td>温度 60℃±3℃,湿度 90%±3%,要求选择时间分别为 96 小时,静、动态（产品点亮）在室温下恢复 2 小时后进行外观,显示功能检查。</td><td>恒温恒湿试验机</td><td>检验外观、功能、抗腐蚀性</td><td rowspan="2">目视/测试架/客户样机/显微镜</td></tr>
<tr><td>2</td><td>高 、低 温冲 击试验</td><td>静态-30℃（30 分钟）∽ 80℃（30 分钟）∽ -30℃（30 分钟），24 个循环，在室温下恢复 2 小时后进行外观,显示功能检查。</td><td>冷热冲击试验机</td><td>检验外观、功能</td></tr>
<tr><td>3</td><td>高 温存 贮试验</td><td>常温70℃+-3℃、宽温80℃+/-3℃、96小时后在室温状态下恢复1 小时在2 小时内完成外观、显示功能检查。</td><td>烤箱</td><td>检验外观、功能</td><td rowspan="2">目视/测试架/客户样机</td></tr>
<tr><td>4</td><td>低 温存 贮试验</td><td>常温-20℃+/-3℃、宽温-30℃+/-3℃、条件的试验箱内保存96小时后在室温状态下恢复1 小时，在2 小时完成外观、显示功能检查，特别注意检查是否有漏液、断线、腐蚀、偏光片不良现象。</td><td>低温冰箱</td><td>检验外观、功能</td></tr>
<tr><td>5</td><td>低温存贮试验（动态）</td><td>常温-20℃+/-3℃、宽温-30℃+/-3℃条件的试验箱内点亮刷屏，过程中每1小时观察一次，检查显示功能，如：异常，卡机，花屏等。特别注意检查是否有漏液、断线、腐蚀、偏光片不良现象。</td><td>低温冰箱</td><td>检验外观、功能</td><td>目视/测试架/客户样机</td></tr>
<tr><td>6</td><td>包 装模 组跌 落试验</td><td>1、跌落重量及自由落体高度：（图二）
 

2、自由落体角度如下：
<table><tr><th>总重量</th><th>自由落体高度</th></tr><tr><td>0-9kg</td><td>92cm</td></tr><tr><td>9-25kg</td><td>76cm</td></tr><tr><td>25-45kg</td><td>53cm</td></tr><tr><td>45-68kg</td><td>46cm</td></tr><tr><td>大于 68kg</td><td>41cm</td></tr><tr><td></td><td></td></tr></table>1） 一角：A角
2） 三菱：A-B, A-D, A-C
3） 六面：面 1，面 2，面 3，面 4，面 5，面 6；</td><td>包装模组跌落架</td><td>测试电性能无异常、外观检验无破损，无脱离现象</td><td>目视/测试架/客户样机</td></tr>
</table>

7	盐雾试验	标准条件:中性盐雾试验（NSS 试验）：5%的氯化钠盐水溶液,溶液 PH 值中性（6.5～7.2），试验温度 35±2℃,盐雾的沉降率在 1～2ml/80cm².h 之间,时间 24h。2.其它特殊要求条件:醋酸盐雾试验(ASS 试验)：5%氯化钠溶液中配入冰醋酸,溶液 PH 值为 3 左右，试验温度 35±2℃,盐雾的沉降率在 1～2ml/80cm².h 之间，时间 24h。	盐雾试验设备	检验外观、功能，盐雾试验结果的判定方法，腐蚀物出现判定法：定性判定，试验后功能测试应 OK，外观观察产品无腐蚀现象产生。	目视/测试架/客户样机/显微镜
8	ESD 抗静电试验	测试架测试状态下试验：接触 4KV,非接触(空气) 8KV 放电测试	抗静电枪（尖头接触放电，圆头空气放电）	检验外观、功能	目视/测试架

6. 光电参数（Optical Characteristics）

The followings are general specifications at the TV070WXQ-NW1.

<Table 1. LCD panel Specifications>

Parameter	Specification	Unit	Remarks
Active Area	94.2(H)*150.72(V)	mm	-
Number Of Pixels	800(H) ×RGB×1280(V)	pixels	-
Pixel Pitch	39.25(H)×RGB×117.75(V)	μm	-
Pixel Arrangement	RGB Vertical stripe	-	Column inversion
Display Mode	Normally Black	-	-
Driver IC	ILI9881C	-	note
Display Colors	16.7M(8bits)	colors	-
Driver Inversion	Column	-	-
Transmittance	5.09%(Typ.) 4.32%(Min.)	-	AG25+Clear
Contrast Ratio	1000:1(Typ.) 800:1(Min.)	-	-
Viewing Angle(CR>10)	85/85/85/85(Typ.) 75/75/75/75(Min.)	deg.	-
Response Time	25(Typ.) 35(Max.)	ms	Tr+Tf
Color Gamut	50%(Typ.) 45%(Min.)	-	CF@C Light
Power Consumption	120	mW	@White

*Note (1) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

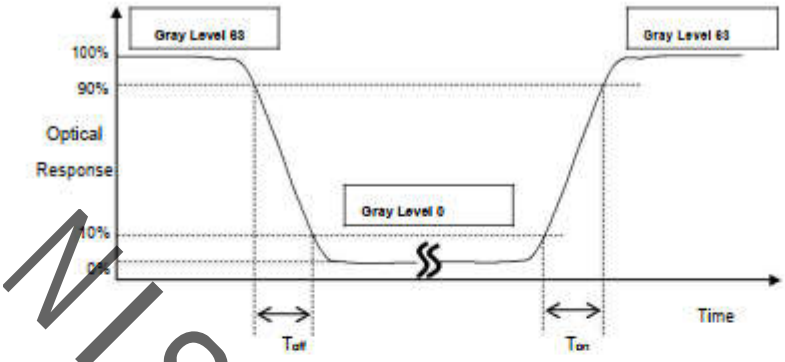
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

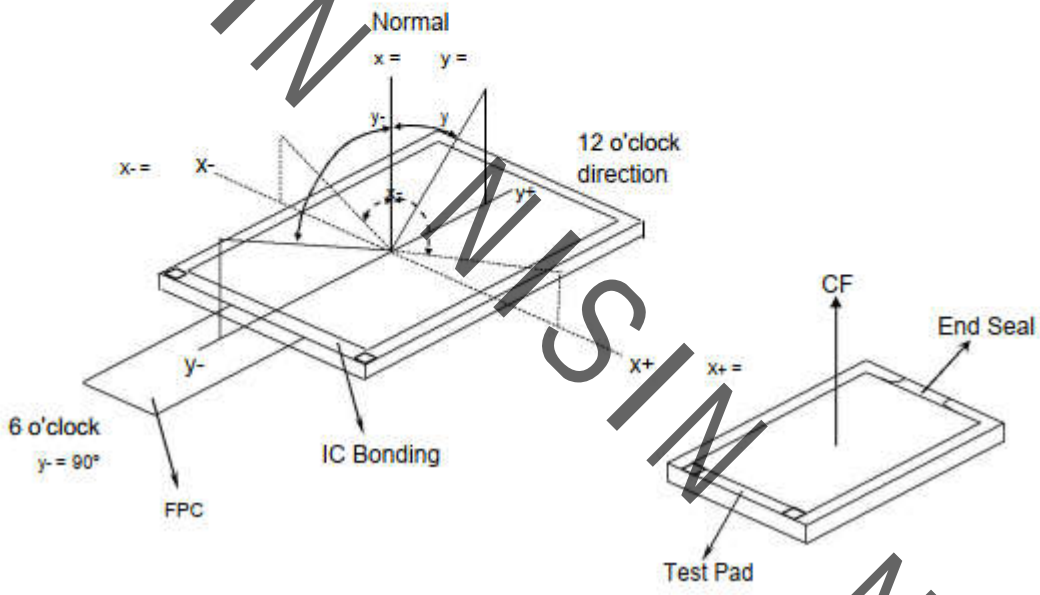
CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (5).

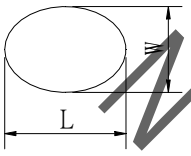
*Note (2) Definition of Response Time (T_{on}, T_{off}):

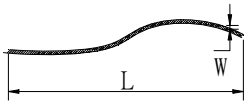
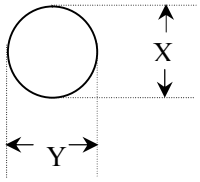


*Note(3) Definition of Viewing Angle



7.检验标准（Inspection standard）

<table>
<tr><td>项目</td><td>不良定义</td><td>不良现象</td><td colspan="3">判定标准</td><td>检验方法</td><td></td></tr>
<tr><td>9.3.1</td><td>外观尺寸</td><td>与图纸尺寸不相符</td><td colspan="3">NG</td><td>卡尺</td><td></td></tr>
<tr><td rowspan="4">9.3.2</td><td rowspan="4">功能</td><td>显示少线</td><td colspan="3">NG</td><td>目视</td><td></td></tr>
<tr><td>无显示</td><td colspan="3">NG</td><td>目视</td><td></td></tr>
<tr><td>显示异常</td><td colspan="3">NG</td><td>目视</td><td>主</td></tr>
<tr><td>TP 功能不良，无触摸</td><td colspan="3">NG</td><td>目视/用手触摸</td><td>主</td></tr>
<tr><td>9.3.3</td><td>点亮产品可见及在 LCD 或 T/P 上有擦拭不掉的点状物</td><td>偏光片刺伤、脏点、圆形物、黑点
 

Φ=(L+W)/2</td><td colspan="3">LCM/总成＞2.4 寸——6.0 寸
Φ≦0.10mm：1、10mm 间距内只允许 3 个；2、显示区只允许 10 个点，超过以上任意一项则 NG
0.1mm＜Φ≦0.15mm：4（TP、屏各允许 2 个）
0.15mm＜Φ≦0.2mm：2（TP、屏各允许 1 个）
Φ＞0.2mm：NG</td><td>目 视(用菲淋卡比对)</td><td>次</td></tr>
<tr><td>9.3.4</td><td>点亮产品可见及在 LCD 或 T/P 上有擦拭不掉的线状物/刮伤</td><td> 
</td><td colspan="3">LCM/总成 0.95 寸——6.0 寸
长(L)≦1mm：宽(W)≦0.03mm：允许个数 2
长(L)≦2mm：0.03＜W≦0.05mm：允许个数 1
长(L)＞2mm：＞0.05mm：NG
两条线毛之间必须距离 5mm 以上（0.95 寸—3.0 寸）.
两条线毛之间必须距离 10mm 以上（3.1 寸—6.0 寸）.</td><td>目视(用菲淋卡比对)</td><td>次</td></tr>
<tr><td>9.3.5</td><td>偏光片气泡</td><td>Φ=（X+Y）/2
 
</td><td colspan="3">尺寸：允许个数
1、Φ≦0.1mm 2、不超过边框 1/3：不计(密集不可)
0.10＜Φ≦0.2mm：1</td><td>在日光台灯下撕起保护膜，距待测物 30cm 目视</td><td>次</td></tr>
</table>

			Φ＞0.2mm	NG		
			0.95 寸-2.4 寸气泡间距大于 5mm 以上 ＞2.4 寸-6.0 寸气泡间距大于 10mm 以上			
9.3.6	T/P 及偏光片凹凸点	T/P:LCD 偏光片上有凹凸点	可视区有水纹（擦拭不掉）拒收 未进入可视区允收，客户装机后不见允收		在同一视角下用样品比对	次
9.3.7	Mura	边框四周或任一侧的色差、较画面深、区域云状不均、固定位置之图形凹陷状、封口部分较画面深的半圆形、一圈圈均匀的色差、线状 mura、黑画面可见因 spacer 聚集产生的 mura、均匀的实斜线、区域性斜线、Driver IC 与 TFT 匹配问题等原因的 mura	1.判定示画面为 128 灰阶画面，用 ND filter 盖住 mura 位置进行判定。 2、ND1.3（ND5%可遮盖不见） 3、双方若有签 限度样品，优先限度样品。		ND filter, 128 灰阶画面	次